processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate,

bonding at least one integrated circuit chip to said interposer element such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element; and

forming a metallization pattern on or within said insulating layer, said metallization pattern being connected with said at least one passive circuit element.

96. (please cancel without disclaimer or prejudice)

REMARKS/ARGUMENTS

Claims 88, 90-95 and 96-123 are currently pending in the above-identified application, with claim 88 being the sole independent claim. Claim 88 has been amended to incorporate the subject matter of claim 96, and claim 96 has been cancelled. Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

Claim 122 stands rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make or use the invention (Office Action, page 2, section 1). In particular, the Office Action states, "[b]y definition alone, an insulating layer does not conduct electricity and therefore all element[s] formed on or in it are passive." This assertion is respectfully traversed. First of all, the Office Action is misquoting the